Periodic Loop Structure for Combining Power FETs

Kimberley W. Eccleston
Dept of Elec. and Comp. Eng., University of Canterbury,
Christchurch, New Zealand
E-mail: kim.eccleston@canterbury.ac.nz

Introduction

Power dividers and combiners are important components in combined power amplifiers. For ease of integration with transistors (or amplifier modules) on a planar circuit, the output ports of the divider and the input ports of the combiner should be aligned in a straight line. When fork or radial power combiners are used, irregular meandering of interconnecting transmission lines is required [1]. Microstrip corporate power combiners [2] and suitably designed tapered microstrip combiners [3], on the other hand, have input ports in a straight line. Most power dividers and combiners are meant to be terminated at all ports with matched loads. When integrating with transistors, matching is required, and this adds to the circuit complexity and size.

In the interests of improving integration of transistors and power combiners and dividers, a number of approaches have been developed such as the dual-fed distributed amplifier [4] and the distributed active transformer [5][6]. The power combiner needs to transform an external load (typically 50 Ω) to a suitable load impedance for the transistors which is low for power FETs. The load-impedance presented to each FET of the dual-fed distributed amplifier is proportional to the number of FETs, N, [4], and inversely proportional to N for the distributed active transformer [5]. The distributed active transformer therefore permits combining of microwave power FETs without needing additional impedance transformers.

The distributed active transformer requires tightly coupled lines and implementation requires a multi-metal-layer technology. In this work we propose an N-way circuit level power combiner for FETs that achieves a 1/N impedance transformation ratio and can be implemented in a single layer microstrip technology.

Proposed Planar Power Combiner

Fig. 1 shows a 4-way version of the proposed power N-way combiner that is driven by 4 equal current sources but with alternating polarity. The input ports are located in a straight line. Extension to N input ports would be evident. The combiner is based upon the rat-race coupler and comprises a cascade of equal sized loops of transmission lines. The load impedance is Z_L, which is typically 50 Ω, and all the transmission lines have a characteristic impedance of Z_{oC}. A distinction needs to be made concerning the input excitations, namely, the input ports of the proposed combiner are driven by drain current sources and not matched sources.

To analyze the combiner, it can be shown that the circuit of Fig. 1 is equivalent to Fig. 2 at the centre frequency. Under the given excitation, the midpoints of the vertical transmission lines are short circuited to earth and Fig. 2 simplifies to Fig. 3, it can be shown that each current source drives into an impedance of Z_{oC}^2/NZ_L at the centre frequency.

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Fig. 4 shows the frequency response of the input impedances of ports 1 to 4 when ports 1 to 4 are equally driven by current sources but with alternating 0° and 180° phase. For the simulation in Fig. 3, Z_L is 50 Ω and Z_{oC} is 50 Ω, and the centre frequency is 1 GHz. At the centre frequency, the input port impedance is 12.5 Ω. If Z_{oC} is 71 Ω, the port input impedance is 25 Ω. If the number of input ports is 6, and Z_{oC} is 71 Ω, the input impedance is 16.8 Ω. These results are consistent with the input impedance given by Z_{oC}^2/NZ_L.

Application of the Proposed Combiner in a Power Amplifier

Fig. 5 shows the integration of a 4-way version of the proposed combiner with four FETs. The FET gates are fed similar to a balanced single-ended dual-fed distributed amplifier [4].

Let us now consider the design of a power amplifier using the Eudyna GaAs FET, FLC057WG. For this FET, the RF output resistance is 121 Ω, the knee voltage is 1 V, the maximum saturation drain current is 200 mA. With a drain supply voltage of 3.6 V, class-A efficiency is maximized when the load is 33 Ω. Under this condition, the load power is 102 mW, and the efficiency is 28 %. The loadline is 26 Ω being the parallel combination of 33 Ω and 121 Ω. When 4 FETs are combined, the load power up to compression is expected to be 408 mW or 26.1 dBm. If the load connected to the combiner is 50 Ω, then Z_{oC} needs to be 81 Ω which is easily realised in microstrip. By contrast, the dual-fed distributed amplifier technique would require a characteristic and load impedance of 16.5 Ω [4].

Harmonic balance simulations were used to assess the feasibility of the amplifier. The FETs were represented by a nonlinear circuit model and included parasitics. Shunt inductors were used to parallel resonate the input and output of each FET at 2 GHz. The drain bias was fed via a quarter-wave stub to the centre of the midpoint of the transmission line immediately connecting the drains of FET2 and FET3.

Simulated load lines showed that the load impedances seen by the FETs at 2 GHz are identical and equal to 29 Ω and this is consistent with the theoretical value of 26 Ω. At the 1 dB gain compression point, the load power is 26 dBm and the power added efficiency is 33 %.

Both the input feed structure and the output power combiner can be realised in a single layer microstrip technology and therefore are amenable to miniaturization methods [7][8]. The artificial transmission lines methodology allows FET input and output parasitic capacitances to be absorbed into the divider and combiner [7].

Conclusion

A combiner constructed from periodic loops of transmission lines has been proposed for specifically combining FETs. The load presented to each FET is inversely proportional to N (the number of FETs) and have sufficiently low impedance for efficient operation of power FETs from a low supply voltage. Feasible values of transmission line characteristic impedance are used, and the combiner circuit is completely planar and therefore can be realized with a single layer microstrip technology.

References

[1] A. A. M. Saleh, "Planar electrically symmetric n-way hybrid power dividers/combiner", *IEEE Trans. on Microwave Theory and Techn.*, Vol. MTT-28, No. 6, pp 555 - 563, June 1980.

[2] J. Zhou, K. A. Morris and M. J Lancaster, "General Design of Multiway Multisection Power Dividers by Interconnecting Two-Way Dividers", *IEEE Trans. on Microwave Theory and Techn.,* Vol. 55, No. 10, pp 2208 - 2215, October 2007.

[3] K. W. Eccleston, Q. C. Sun and S. P. Yeo, "Tapered microstripline power combiners with colinear input ports", *Microwave and Optical Technology Letters*, Vol. 15, No. 6, pp339 - 342, 20 August 1997.

[4] K. W. Eccleston and O. Kyaw, "Analysis and Design of Class-B Dual-Fed Distributed Power Amplifiers", *IEE Proceedings. H, Microwaves, Antennas and Propagation*, Vol. 151, No. 2, pp 104-108, April 2004.

[5] I. Aoki, S. D Kee, D. B. Rutledge and A. Hajimiri, "Distributed Active Transformer - A New Power-Combining and Impedance-Transformation Technique", ", *IEEE Trans. Microwave Theory and Techn.*, vol. 50, no. 1, pp 316 - 331, Jan 2002.

[6] S. Kim, *et al*, "An Optimized Design of Distributed Active Transformer", *IEEE Trans. Microwave Theory and Techn.*, vol. 53, no. 1, pp 380 - 388, Jan 2005.

[7] K. W. Eccleston, "Compact Efficient Dual-Fed Distributed Power Amplifier", *IEEE Trans. on Microwave Theory and Techn.*, Vol 53, No 3, pp 825 - 831, March 2005.

[8] W.-L. Chen and G.-M. Wang, "Design of Novel Miniaturized Fractal-Shaped Branchline Couplers", 2007 Asia-Pacific Microwave Conference, pp 2155 - 2158.

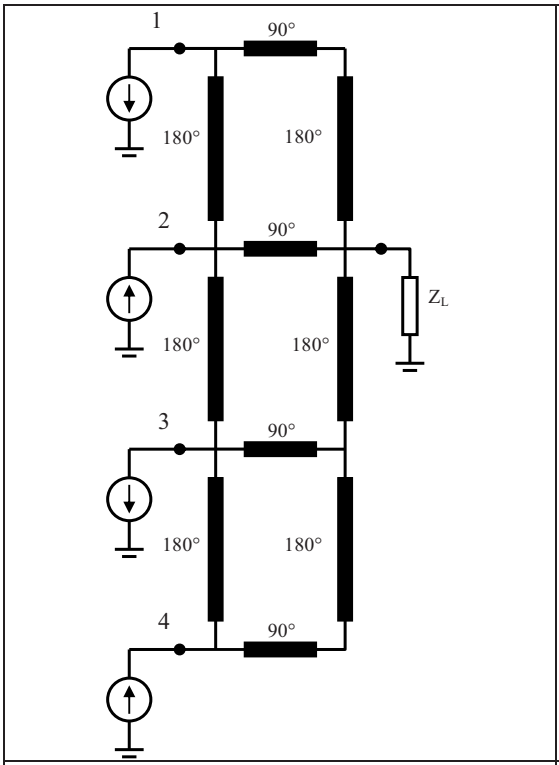

Figure 1. Proposed 4-way power combiner showing excitation current sources and load. All transmission line have a characteristic impedance of Z_{oC}.

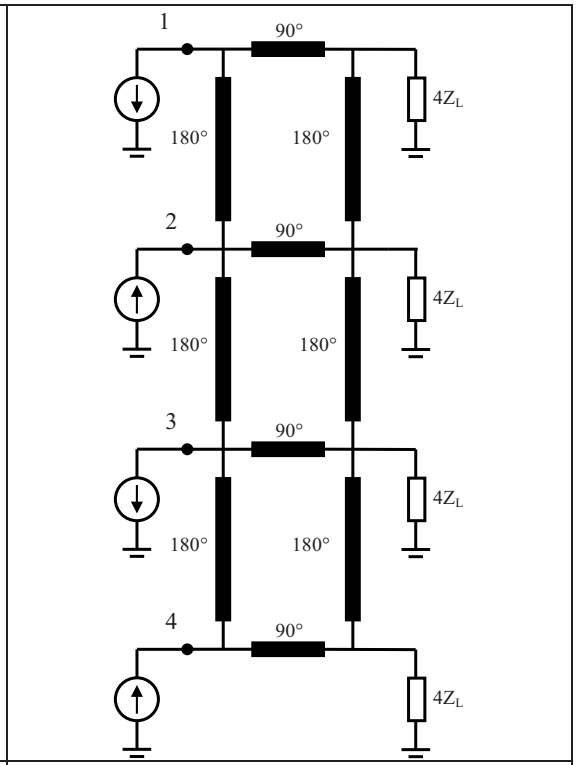

Figure 2. Equivalent circuit of the 4-way combiner. All transmission lines have a characteristic impedance of Z_{oC}.

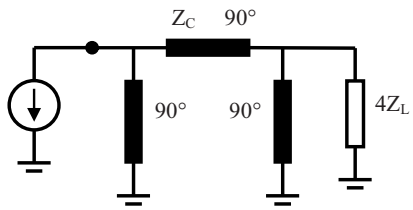

Figure 3. Odd mode equivalent circuit.

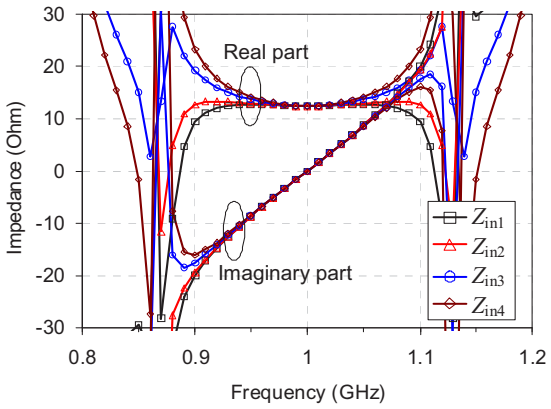

Figure 4. Input impedances of ports 1 to 4 when ports 1 and 4 are equally driven but with alternating 0° and 180° phase. Z_L and Z_{oC} are 50Ω.

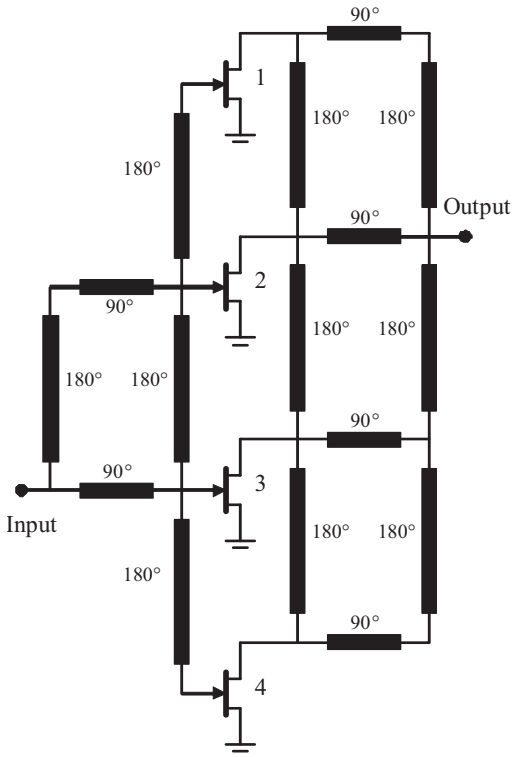

Figure 5. Schematic of a 4-FET power amplifier using the proposed power combiner.